What is claimed is:

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~~1.~~ A ~~shift register circuit, comprising:~~

a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;

a clock signal line transmitting a clock signal; and

a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein

potentials at nodes of the plurality of latch circuits vary in accordance with the pulse signal transferred;

the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits;

in at least part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency which is lower than in a normal operation period and which gradually increases; and

upon power-on, at least one of the switching circuits electrically disconnects at least one corresponding latch circuit from the clock signal line.

2. A shift register circuit, comprising:

a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;

a clock signal line transmitting a clock signal; and

a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein

at least one of the switching circuits electrically disconnects at least one of the plurality of latch circuits from the clock signal line at regular intervals.

3. The shift register circuit according to claim 2, wherein:

potentials at nodes of the plurality of latch circuits vary in accordance with the pulse signal transferred;

the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits; and

in at least part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency lower than in a normal operation period.

4. The shift register circuit according to claim 3, wherein the frequency of the clock signal gradually increases in said at least part of the period.

5. The shift register circuit according to claim 1, wherein the frequency of the clock signal in said at least part of the period is from 1/2 to 1/16 of a frequency of the clock signal in the normal operation period.

6. The shift register circuit according to claim 3, wherein the frequency of the clock signal in said at least part of the period is from 1/2 to 1/16 of a frequency of the clock signal in the normal operation period.

7. The shift register circuit according to claim 4, wherein the frequency of the clock signal in said at least a part of the period is from 1/2 to 1/16 of a frequency of the clock signal in the normal operation period.

8. The shift register circuit according to claim 1, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.

9. The shift register circuit according to claim 2, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and

initializing an internal node of the latch circuit in response to the initialization signal.

10. The shift register circuit according to claim 1, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

11. The shift register circuit according to claim 2, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

12. The shift register circuit according to claim 1, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

13. The shift register circuit according to claim 2, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

14. The shift register circuit according to claim 1, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit

further comprises a level shifter changing the amplitude of the clock signal received from outside.

15. The shift register circuit according to claim 2, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

16. An image display device of active matrix type, comprising:

a plurality of pixels arranged in a matrix form;

a data signal line supplying video data to be written to one of the plurality of pixels;

a scan signal line for controlling the writing of the video data to one of the plurality of pixels;

a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and

a scan driver supplying a pulse signal to the scan signal line in synchronization with a timing signal,

at least one of the data driver and the scan driver comprising the shift register circuit according to claim 1.

17. An active matrix image display device, comprising:

a plurality of pixels arranged in a matrix form;

a data signal line supplying video data to be written to one of the plurality of pixels;

a scan signal line for controlling the writing of the video data to one of the plurality of pixels;

a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and

a scan driver supplying a pulse signal to the scan signal line in synchronization with a timing signal,

at least one of the data driver and the scan driver comprising the shift register circuit according to claim 2.

18. The image display device according to claim 16, wherein the data driver has the shift register circuit, and initializes the potential level at each of internal nodes of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

19. The image display device according to claim 17, wherein the data driver has the shift register circuit, and initializes the potential level at each of internal nodes of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

20. The image display device according to claim 16, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels are also formed.

21. The image display device according to claim 17, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels are also formed.

22. The image display device according to claim 20, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

23. The image display device according to claim 21, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

24. The image display device according to claim 22, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600°C or lower.

25. The image display device according to claim 23, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600°C or lower.

26. A driving method for an active-matrix liquid crystal display device, in which a pixel electrode is connected to a data signal line by a switching device based on a control signal supplied from a scan driver, and a data signal output from a data driver is supplied to the pixel electrode through the data signal line, so that a picture based on the data signal is displayed by a pixel matrix, wherein:

in performing black display in an upper black display area provided in an upper position of a screen and in a lower black display area provided in a lower position of the screen, a stabilization period is provided, in one vertical scan period, between a first black display period in which black display is performed in the upper black display area and a video display period in which video display is performed in a video display area below the upper black display area and between the video display period and a second black display period in which black display is performed in the lower black display area below the video display area, said stabilization period being a period in which a frequency of a clock signal for operating a shift register included in the data driver is made lower than a frequency of the clock signal in the video display period such that a potential level at an internal node of the shift register is stabilized.

27. The driving method according to claim 26, wherein a frequency of the clock signal of the data driver in the stabilization period is from 1/2 to 1/32 of a frequency in the video display period.

28. The driving method according to claim 26, wherein in the first and second black display periods, a frequency of a clock signal for operating a shift register circuit included in the scan driver is made higher than a frequency in the video display period, irrespective of a horizontal blanking period, and an analog switching section included in the data driver to sample the data signal is always placed in an on state.

29. The driving method according to claim 28, wherein the frequency of the clock signal for operating the shift register circuit in the scan driver in the first and second black display periods is 1.5 - 10 times as high as the frequency in the video display period.

30. The driving method according to claim 26, which is used for a liquid crystal display device wherein at least one of a scan driver and a data driver has a shift register which comprises a plurality of latch circuits connected in series to transfer a pulse signal from one to another in synchronization with a clock signal, and the shift register is designed such

that the clock signal is supplied to only a latch circuit in which a pulse of the pulse signal is present and its neighboring latch circuits.

31. The driving method according to claim 26, which is used for a liquid crystal display device wherein at least one of a scan driver and a data driver has a shift register which comprises a plurality of latch circuits connected in series to transfer a pulse signal from one to another in synchronization with a clock signal, and the shift register is designed such that the clock signal is supplied to all the latch circuits.

32. The driving method according to claim 26, which is used for a liquid crystal display device wherein at least one of a scan driver and a data driver is formed on a substrate on which pixel electrodes are also formed.

33. The driving method according to claim 26, which is used for a liquid crystal display device wherein a switching device for connecting a pixel electrode to a data signal line is made of a polysilicon thin-film transistor.

34. The driving method according to claim 33, wherein the switching device has been formed on a glass substrate at a temperature of 600 °C or lower.

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